Process for forming a dual damascene structure

FIELD OF THE INVENTION

The invention is generally related to the field of semiconductor devices and fabrication and more specifically to a method for forming a dual damascene structure.

BACKGROUND OF THE INVENTION

To increase the operating speed, high performance integrated circuits use copper interconnect technology along with low dielectric constant dielectrics. Currently the dual damascene method is the most widely used method for forming copper interconnects. A typical dual damascene process is illustrated in Figures 1(a) - 1(c). As shown in Figure 1(a), a first etch stop layer is formed over a dielectric layer 10 and a copper line 20. A first dielectric layer 40, a second etch stop layer 50, and a second dielectric layer 55 are formed over the first etch stop layer. A patterned layer of photoresist is then formed and used to pattern the etching of the first trench 57. Following the etching of the first trench 57, a backside anti-reflective coating (BARC) layer 60 is formed. During the formation of the BARC layer 60, additional BARC material 65 is formed in the trench 57. The additional BARC

material 65 is necessary to protect the bottom surface of the trench during the etching of the second trench 58. This is illustrated in Figure 1(b). A portion of the additional BARC 65 is removed during the etching process. Following the etching of the second trench 58, trench liner material is formed 80 and copper 90 is used to fill both trenches as illustrated in Figure 1(c).

There are a number of important issues concerning the use of the additional BARC 65 to mask the trench. Some of the more important of these are non-uniformity in dense and isolated structures, punching through the first etch stop layer 30 during the etching process, defects caused by the BRAC material etc. These is therefore a need for an improved process that overcomes the issues associated with the use of the BARC trench masking material 65.

SUMMARY OF THE INVENTION

The present invention describes a process for forming dual damascene structures. In particular, a first dielectric layer is formed over a silicon substrate containing one or more electronic devices. A first etch stop layer is then formed over this first dielectric layer and a second dielectric layer is then formed over the first etch stop layer. A silicon oxynitride anti-reflective coating layer is then formed over the second dielectric layer and a first trench is etched to a first depth in the second dielectric layer and the first dielectric layer. A second trench is etched in the second dielectric layer while simultaneously etching the first trench in the first dielectric layer.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGURES 1(a) - 1(c) are cross-sectional diagrams illustrating the prior art.

FIGURES 2(a) - 2(d) are cross-sectional diagrams illustrating an embodiment of the instant invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described with reference to Figures 2(a) - 2(d). It will be apparent to those of ordinary skill in the art that the benefits of the invention can be applied to other structures where a dual damascene process is utilized.

The requirement of higher clock rates has lead to the use of copper to form the metal interconnect lines in integrated circuits. In addition to the use of copper, dielectric layers such as organosilicate glass (OSG) (dielectric constant $\underset{\sim}{}$2.6) and florosilicate glass (FSG) are currently being used to take advantage of the lower dielectric constant of such materials compared to silicon dioxide. In an embodiment of the instant invention, a first etch stop layer 130 is formed over a copper layer 120 and a dielectric layer 100 as shown in Figure 2(a). The dielectric layer 100 is formed over a silicon substrate which contains one or more electronic devices such as transistors, diodes, etc. These electronic devices will typically be part on an integrated circuit. The dielectric layer 100 may formed over various portions of an integrated circuit. The copper layer 120 represents a portion of the copper interconnect of the integrated circuit. The first

etch stop layer 130 may comprise silicon nitride (SiN), silicon carbide (SiC), or any suitable material. Following formation of the first etch stop layer 130, a first dielectric film 140 is formed over the etch stop layer 130. In an embodiment of the instant invention this first dielectric layer 140 comprises florosilicate glass (FSG) which has a dielectric constant of about ????. In addition to FSG any suitable dielectric material may be used to form the first dielectric layer 140. Following the formation of the first dielectric layer 140, a second etch stop layer 150 may or may not be formed. This second etch stop layer 150 comprises a material selected from the group consisting of silicon nitride (SiN), silicon carbide (SiC), or any combination of layers of these or other suitable materials. Following the formation of the second etch stop layer 150, a second dielectric layer is formed. In an embodiment of the instant invention this second etch stop layer comprises FSG, OSG or any suitable dielectric material. Following the formation of the second dielectric layer 160, a layer of anti-reflective coating (ARC) 170 is formed as shown in Figure 2(a). In an embodiment of the instant invention this ARC layer 170 comprises silicon oxynitride. An important property of the ARC layer 170 is that no light be reflected during the photolithographic process. Such an ARC film can

be formed using silicon oxynitride with the following atomic percentages, silicon (30% - 55%), oxygen (20% - 50%), nitrogen (2% - 17%), and hydrogen (7% - 35%). Following the formation of the ARC layer 170, a photoresist layer is formed and patterned 180. The ARC layer 170, the second dielectric layer 160 and the second etch stop layer 150 are etched using a multi-step etch process to form a first trench 185 as illustrated in Figure 2(a). In an embodiment of the instant invention the silicon oxynitride layer can be etched using a CF_4 based plasma etch process. In particular a 300A to 2000A silicon oxynitride film can be etched using CF_4 with flow rates of 50sccm - 120sccm, oxygen with flow rates of 1sccm - 9sccm, argon with flow rates of 200sccm - 500sccm, and power of about 1000W to 2000W. One advantage of using the silicon oxynitride film is that thinner layers of photoresist (i.e. less than 3000A) can be used. This leads to improved resolution over the thicker resist films necessary in current processes. For cases where FSG is used to form the second dielectric layer 160, an argon (200sccm - 400sccm), CH_2F_2 (10sccm - 35sccm), and oxygen (9sccm - 34sccm) based plasma etch process can be used with power levels of approximately 1000W. Finally to etch through the second etch stop layer 150, a C_5F_8 (5sccm - 13sccm), argon (300sccm - 650sccm), and

oxygen (4sccm - 13sccm) etch process with a power level of approximately 1500W can be used. The depth of the first trench 187 is variable. The embodiment represented in Figure 2(a) shows the bottom surface of the trench below the second etch stop layer. In general the required depth of the first trench depends on the thickness of the dielectric layers 140 and 160 and the required depth of the second trench.

Following the formation of the first trench 185, the remaining photoresist film 180 is removed and another patterned photoresist film is formed 190 which will be used to define the width of the second trench. This is illustrated in Figure 2(b). Using the photoresist film as an etch mask, the exposed regions of the ARC layer 170 is etched. For the case where a silicon oxynitride ARC layer is used the layer can be etched using a CF_4 based plasma etch process. In particular a 300A to 2000A silicon oxynitride film can be etched using CF_4 with flow rates of 50sccm - 120sccm, oxygen with flow rates of 1sccm - 9sccm, argon with flow rates of 200sccm - 500sccm, and power of about 1000W to 2000W. During the subsequent etching of the dielectric layers 160 and 140 the ARC layer will serve as a hardmask. Dielectric layers 160 and 140 are then etched

simultaneously with a second trench 195 being formed in the second dielectric layer 160 and the first trench 185 etched in the first dielectric layer 140 as shown in Figure 2(c). The etching of the second trench 195 will stop on the second etch stop layer 150 (if present), and the etching of the first trench 185 in the first dielectric layer 140 will stop on the first etch stop layer 130.

During the formation of the second trench 195 in the second dielectric layer 160, the etching of the first trench 185 is completed in the first dielectric layer. The first etch stop layer 130 beneath the first dielectric layer 140 is therefore not exposed to the entire second trench etching processes. This eliminates the need for the BARC protective layer currently used in the art.

Following the formation of both trenches (185 and 195) the exposed region of the first etch stop layer 130 is removed and a liner film 200 is formed as shown in Figure 2(d). The formation of the liner film is followed by a copper deposition and chemical mechanical polishing process which results in the copper layer 210 shown in Figure 2(d). Typically the copper layer 210 is formed by first forming a

thick layer of copper followed CMP processes to remove the excess copper.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.